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42390P13736

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Glew, et al for Intel Corporation	Examiner: Pyzocha, Michael J.
Serial No.: 10/039,961	Art Unit: 2137
Filing Date: December 31, 2001	
For: PROCESSOR SUPPORTING EXECUTION OF AN AUTHENTICATED CODE INSTRUCTION	

CERTIFICATE OF MAILING/TRANSMISSION

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AMENDED APPEAL BRIEF

42390P13736 PATENT

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEAL AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-2 (Rejected).

Claim 3 (Canceled).

Claims 4-6 (Rejected).

Claim 7 (Canceled).

Claims 8-9 (Rejected).

Claims 10-11 (Withdrawn).

Claims 12-18 (Rejected).

Claims 19-21 (Withdrawn).

Claims 22-23 (Rejected).

Claim 24 (Canceled).

Claims 25-26 (Withdrawn).

Claims 27-29 (Canceled).

Claims 30-31 (Withdrawn).

Claims 32-39 (Canceled).

Claims 1-2, 4-6, 8-9, 12-18, and 22-23 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

All amendments have been entered.

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SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claim is read on one of many possible embodiments without limiting the claim.

1. A processor (Page 14, paragraph 0040, line 1) comprising

memory (Page 14, paragraph 0040, lines 6 and 10; Fig. 3, 360);

decode logic (Pages 14-17, paragraph 0040, line 5, paragraph 0041, paragraphs 0043-0045; Fig. 3, 340) to receive a launch instruction; and

one or more execution units (Pages 14-15, paragraph 0040, line 3, paragraph 0042; Fig. 3, 370) to execute the launch instruction by loading an authenticated code module into the memory (Pages 20-21, paragraph 0055), locking the memory (Page 21, paragraph 0056), retrieving a key (Page 21, paragraph 0057, lines 4-5), authenticating the authenticated code module stored in the memory using the key (Pages 21-22, paragraph 0057, lines 6-11), and initiate execution of the authenticated code module stored in the memory (Page 23, paragraph 0061).

At this point, no issue has been raised that would suggest that the words in the claims have any meanings other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claim 1 is unpatentable over U.S. Patent No. 6,651,171 ("England") in view of U.S. Patent No. 6,704,872 ("Okada").

ARGUMENT

A. Is claim 1 unpatentable over England in view of Okada?

It is respectfully argued that the combination of England and Okada is improper. The examiner argues that the motivation to apply Okada to England is to provide a processor with a function to prevent the illegal execution of a program, which is an object of Okada (see column 3, lines 34 to 38). This object, therefore, is allegedly fulfilled by the disclosure of Okada. Therefore, the authentication operation of Okada is to limit the right to use a specific software program to a single processor (i.e., to authenticate the processor). In contrast, England has an entirely different object, which is to hide the execution of curtained code from the normal operation of a system (see column 3, lines 36-44), and the authentication operation of England is to authenticate programs (see column 3, lines 60-64). Combining Okada and England would do nothing to help Okada prevent the illegal execution of a program or to help England hide the execution of curtained code from the normal operation of a system. Therefore, there is no motivation to combine Okada and England.

More specifically, the examiner argues that England describes loading an authenticated code module into memory and locking the memory. Locking the memory, according to England, is disabling all accesses to memory apart from those initiated by the processor executing authorized code (see column 11, lines 40-43). There would be no reason to do this in connection with preventing the illegal execution of a program by a processor. The program would be accessible for execution by the processor, legally or illegally. England is clearly not related to preventing the illegal execution of a program.

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Therefore, the combination of Okada and England is improper and withdrawal of the rejections based on their combination is respectfully requested.

* * *

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue. Please charge any necessary fees, including extension fees, to our Deposit Account No. 50-0221.

Respectfully submitted,

Date: May 12, 2010

Thomas R. Lane
Registration No. 42,781

CLAIMS APPENDIX

The claims on appeal are:

1. A processor comprising

memory;

decode logic to receive a launch instruction; and

one or more execution units to execute the launch instruction by loading an authenticated code module into the memory, locking the memory, retrieving a key, authenticating the authenticated code module stored in the memory using the key, and initiate execution of the authenticated code module stored in the memory.

2. The processor of claim 1 further comprising a cache memory that provides the memory.

4. The processor of claim 2 wherein the execution units lock the cache memory to prevent replacement of lines of the authenticated code module stored in the cache memory.

5. The processor of claim 1 wherein the execution units lock the memory to prevent other processors from altering the authenticated code module stored in the memory.

6. The processor of claim 1 wherein the decode logic is also to generate one or more opcodes for the launch instruction, wherein the execution units authenticate and execute the authenticated code module in response to executing the one or more opcodes.

8. The processor of claim 1, wherein the execution units retrieve the key specified by one or more operands of the launch instruction.

9. The processor of claim 1, wherein the execution units, in response to the launch instruction, retrieve the key from a chipset.

12. The processor of claim 1, wherein the execution units, in response to the launch instruction, decrypt at least a portion of the authentication module stored in the memory.

13. The processor of claim 1, wherein the execution units, in response to the launch instruction, decrypt at least a portion of the authentication module to obtain a digest value, and determine whether the authentication module is authentic based upon the digest value.

14. The processor of claim 1, wherein the execution units, in response to the launch instruction, obtain a digest value for the authentication code module, generate a computed digest value from at least a portion of the authenticated code module, and determine that the authenticated code module is authentic in response to the digest value and the computed digest value having a predetermined relationship.

15. The processor of claim 1, wherein the execution units, in response to the launch instruction, RSA-decrypt a signature of the authentication code module to obtain a digest value from the signature, perform a SHA-1 hash on the authenticated code module to generate a computed digest value, and determine that the authenticated code module is authentic in response to the digest value and the computed digest value being equal.

16. The processor of claim 1, wherein the execution units initiate execution of the authenticated code module only if the authenticated code module is determined to be authentic.

17. The processor of claim 16, wherein the execution units generate an error code in response to determining that the authenticated code module is not authentic.

18. The processor of claim 17, wherein the execution units generate a trap in response to determining that the authenticated code module is not authentic.

22. The processor of claim 1, wherein the execution units authenticate and initiate execution of the authenticated code module stored in the memory in response to executing microcode associated with the launch AC instruction.

23. The processor of claim 1, embodied in a machine readable medium.

EVIDENCE APPENDIX

None.

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RELATED PROCEEDINGS APPENDIX

None.